

REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

Public Reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comment regarding this burden estimates or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188,) Washington, DC 20503.

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE 31 March 2003	3. REPORT TYPE AND DATES COVERED Final Technical Report 1 July 1999 – 30 June 2002	
4. TITLE AND SUBTITLE Exploratory Develop of SiC Bipolar Transistors and GaN Heterojunction Bipolar Transistors for High-Power Switching Applications		5. FUNDING NUMBERS N00014-99-1-0938	
6. AUTHOR(S) Professor James A. Cooper, Jr.			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) School of Electrical and Computer Engineering Purdue University, 465 Northwestern Ave. West Lafayette, IN 47907-2035		8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES) Office of Naval Research 800 North Quincy Street Ballston Centre Tower One Arlington, VA 22217		10. SPONSORING / MONITORING AGENCY REPORT NUMBER	
11. SUPPLEMENTARY NOTES			
12 a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution unlimited.		12 b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) Homojunction bipolar transistors (BJTs) have been designed, fabricated, and characterized in 4H-SiC. Devices optimized for high current gain have betas as high as 55, a new record for SiC BJTs. Devices optimized for blocking voltage exhibit blocking voltages of 3,200 V, again a new record for SiC BJTs. For the high-gain devices, the critical parameter is the base doping, which must be high enough to prevent punchthrough, while low enough to achieve a high emitter injection efficiency. The optimum value in these devices is a doping of about $1 \times 10^{17} \text{ cm}^{-3}$ at a base thickness of 1 μm . Another critical parameter is the lateral spacing between the edge of the emitter and the implanted P+ region used to form the base contact. This spacing needs to be at least 3 μm in order to minimize recombination of injected minority carriers at defect sites in the implanted region. The high blocking voltage devices are fabricated on a 50 μm collector drift region, doped $8 \times 10^{14} \text{ cm}^{-3}$ with nitrogen. Edge termination is provided by a 100 μm wide single-zone aluminum ion-implanted junction termination extension (JTE).			
14. SUBJECT TERMS Bipolar transistors, bipolar junction transistors, BJTs, heterojunction bipolar transistors, HBTs, silicon carbide, SiC.		15. NUMBER OF PAGES 15	
		16. PRICE CODE	
17. SECURITY CLASSIFICATION OR REPORT UNCLASSIFIED	18. SECURITY CLASSIFICATION ON THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT UL
NSN 7540-01-280-5500			

Standard Form 298 (Rev.2-89)
Prescribed by ANSI Std. Z39-18
298-102

418

096

Exploratory Development of
SiC Bipolar Transistors and
GaN Heterojunction Bipolar Transistors
for High-Power Switching Applications

Final Technical Report

31 March 2003

Submitted to:

Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5000

20030418
096

Submitted by:

James A. Cooper, Jr.
School of Electrical and Computer Engineering
Purdue University, West Lafayette, IN 47906-1285

1. Introduction and Background

Several studies [1-3] have indicated that SiC bipolar junction transistors (BJTs) may be the superior power switching device for blocking voltages between 3 - 5 kV and on-state current densities between 200 - 500 A/cm². As blocking voltage increases, BJTs have an advantage over MOSFETs because the forward-biased collector-base junction provides conductivity modulation of the drift region, reducing specific on-resistance. BJTs also have an advantage over IGBTs and GTOs because the BJT does not introduce a forward-biased diode drop into the current path. In SiC, the diode drop is about 2.8 V, resulting in significant on-state power dissipation. At very high current densities (well above 500 A/cm²), the GTO has the lowest static power dissipation because of its greater conductivity modulation. However, the GTO exhibits higher switching loss than the BJT, and therefore is at a significant disadvantage for high-frequency switching applications.

Historically, silicon BJTs were the first power switching devices, but they were eventually replaced by power MOSFETs and later by IGBTs. Two of the problems with silicon BJTs were their low current gain and their limited safe operating area (SOA) due to "second breakdown". Because of the 10x higher breakdown field in SiC, SiC BJTs avoid the fatal shortcomings of silicon BJTs. First, the higher breakdown field allows the collector drift region and base to be much narrower for a given blocking voltage, resulting in higher current gain. Second, SiC BJTs simply do not suffer from second breakdown. Second breakdown occurs under high-level injection conditions when minority carriers injected into the collector drift region cause the net charge density to reverse polarity, shifting the peak electric field from the base edge of the drift region to the sub-collector edge (the N-/N+ junction). Avalanche multiplication then occurs in this high-field region, feeding holes back into the base where they act as base current, increasing the collector current and causing runaway. At a blocking voltage of 4.5 kV, the critical current density for second breakdown in a silicon BJT is about 30 A/cm², whereas in a SiC BJT it is over 6200 A/cm² [1]. Clearly, second breakdown is not an issue in SiC.

Ideally, the performance of SiC BJTs, power MOSFETs, and GTOs should be compared in a three-dimensional parameter space defined by blocking voltage, on-current density, and switching frequency. No one has done such a thorough comparison as yet. However, recent calculations performed by Huang and Zhang [1] provide some insight. Huang and Zhang determined the locus of constant power dissipation for the SiC MOSFET, BJT, and GTO as a function of on-current and switching frequency at a constant blocking voltage of 4.5 kV. The power dissipation chosen for comparison was the package limit of 1.3 kW/cm². For current densities below 200 A/cm², the MOSFET has the highest permissible switching frequency. For current densities between 200 - 450 A/cm², the BJT has the highest permissible frequency, and

above 450 A/cm^2 the GTO is highest. However, the maximum switching frequency the GTO can achieve is less than 500 Hz because of minority carrier charge storage in the drift region. For comparison, the BJT can switch at 8 - 50 kHz, and the MOSFET can switch at 50 - 300 kHz. The basic conclusion is that **for blocking voltages between about 3 - 5 kV, the MOSFET is limited to low current densities and the GTO is limited to low switching frequencies. The BJT is the superior device in this blocking voltage range.**

As blocking voltage is reduced, the MOSFET tends to win over a broader range of current densities. The MOSFET is clearly the best device at low current densities ($< 200 \text{ A/cm}^2$), with the crossover current density increasing as the blocking voltage is reduced. The GTO is superior at very high current densities ($> 500 \text{ A/cm}^2$), but then only at low switching frequencies.

Physically, the BJT achieves lower resistive drops than the MOSFET at a given blocking voltage because the forward-biased collector-base junction injects holes into the collector drift region, lowering its resistance by conductivity modulation. Also, since the BJT has an *even* number of pn junctions, there is no forward-biased diode drop to dissipate on-state power, unlike the IGBT and GTO. As a result, **the BJT has lower on-state power dissipation than the GTO, IGBT, or MOSFET for current densities up to 500 A/cm^2 at 4.5 kV.** Huang and Zhang's simulations show that the BJT also has lower switching loss than the GTO (by an order of magnitude), although its switching loss is higher than the MOSFET.

In this project we have designed, fabricated, and characterized 4H-SiC homojunction BJTs with record high current gains $\beta > 50$, and BJTs with the highest blocking voltage yet reported, $\text{BV}_{\text{CEO}} > 3,200 \text{ V}$. These results will be described in the following sections.

References

- [1] A. Q. Huang and B. Zhang, "Comparing SiC Switching Power Devices: MOSFET, NPN Transistor, and GTO Thyristor," submitted to *Solid-State Electronics*, April, 1999.
- [2] A. K. Agarwal, private communication, ONR Wide Bandgap Bipolar Workshop, January 1999.
- [3] T. P. Chow, ONR/MURI program review, January 1999.

2. High Current-Gain 4H-SiC NPN Bipolar Junction Transistors

Device Fabrication

An interdigitated finger structure with 28 μm pitch is used for the 4H-SiC npn bipolar transistors. The emitter, base, and collector layers are epitaxially grown on an n+ substrate. The top n+ emitter layer is 1 μm thick, doped $1 \times 10^{19} \text{ cm}^{-3}$ with nitrogen. The p-type base layer is also 1 μm thick, doped $1.2 \times 10^{17} \text{ cm}^{-3}$ with aluminum. The n- collector layer is 20 μm thick, doped $2.4 \times 10^{15} \text{ cm}^{-3}$ with nitrogen. Emitter fingers and base mesas are defined by reactive ion etching in SF₆. Aluminum is implanted to form p+ contact regions along each base finger. A second aluminum implant creates a junction termination extension (JTE) [6] around the base mesa with dose/energy of $1 \times 10^{12}/40$, $2 \times 10^{12}/100$, $3 \times 10^{12}/200$, and $5 \times 10^{12}/350 \text{ keV/cm}^2$. Implants are activated at 1600 °C for 30 minutes in argon. The surface is passivated by an MOS-quality thermal oxide grown in wet oxygen at 1150 °C for 2.5 hours, followed by an in-situ argon anneal at 1150 °C for 1 hour and a re-oxidation anneal in wet oxygen at 950 °C for 2 hours. P-type base contact metals are 30 nm titanium followed by 100 nm aluminum. N-type emitter and collector contacts are 100 nm nickel. All contacts are annealed at 1000 °C for 2 minutes in argon. A 0.8 μm gold layer is deposited as the top interconnect metal, and 0.5 μm of gold is deposited on the back for the collector contact. A cross section of the device structure is shown in Fig. 1.

Results and Discussion

Both n-type and p-type contacts exhibit ohmic characteristics with contact resistivity of 1.8×10^{-5} and $9.0 \times 10^{-4} \text{ ohm}\cdot\text{cm}^2$ measured from TLM structures. Figure 2 shows the on-state characteristics of a BJT with active area of 1.05 mm² and finger length of 350 μm at room temperature, measured using a Tektronix 371A curve tracer. The base current is pulsed to avoid heating the device under test. This device carries 2 A (190 A/cm²) at a forward voltage of 5 V and base current of 50 mA. The DC current gain in the forward active region is around 55, and the specific on-resistance is 26 mΩ·cm², about 5 to 6 times higher than the theoretical unipolar value for the collector epilayer. This device has BV_{CEO} of 500 V and BV_{CBO} of 700 V, only 20% of the theoretical value for this collector epilayer. We attribute

the low blocking voltage to punchthrough in the base caused by aluminum spiking during the high-temperature ohmic contact anneal. Prior to the contact anneal, BV_{CBO} was greater than 1,900 V on a test diode. Figure 3 shows current gain β versus collector current density J_C of a small device (active area = $55 \times 55 \mu\text{m}^2$). This device maintains β above 50 at current density above 700 A/cm^2 .

Small BJT test devices are used to investigate the effect of the p+ base contact implant on the current gain. Figure 4 shows the averaged value of current gain on more than 30 devices at each data point. Also shown in the figure are similar result obtained in a previous experiment [7], which used the same fabrication technology and emitter/base design. The only difference is the base dose Q_B . Both curves show that as the spacing between the p+ base contact implant and the edge of the emitter finger decreases, the current gain decreases. We believe this is due to recombination at defect sites introduced by the p+ implant. When the p+ implant is self-aligned to the emitter finger, i. e. the gap is zero, current gain is dominated by the recombination in the base. The base dose Q_B has hardly any effect on the current gain in this case. When the p+ implant is more than $3 \mu\text{m}$ away from the emitter, the recombination in the base region is reduced. In this case the current gain is dominated by emitter injection efficiency and is inversely proportional to ionized dose [8]

$$\beta \sim 1/Q_B^{-1}$$

The current gain doubles when the base dose is reduced by nearly half.

Conclusions

We have fabricated 4H-SiC BJTs with current gain of 55, the highest values yet reported. The surface is passivated by an MOS gate-quality oxide to reduce surface recombination. We compare the current gain corresponding to different base doses in different devices, and find that the gain is sensitive to the spacing between the p+ base contact implant and the edge of the emitter finger. The current gain is limited by emitter injection efficiency if the spacing is greater than $3 \mu\text{m}$, and by recombination at the base contact implant if the spacing is less than $1 \mu\text{m}$.

References

- [1] T. P. Chow, V. Khemka, J. Fedison, N. Ramungul, K. Matocha, Y. Tang, and R. J. Gutmann, "SiC and GaN bipolar power devices," *Solid-State Electronics*, vol. 44, pp. 277-301, 2000.
- [2] A. Q. Huang, and B. Zhang, "The Future of Bipolar Power Transistors," *IEEE Trans. on Electron Devices*, vol. 48, pp. 2535-2543, Nov. 2001.
- [3] A. Galeckas, J. Linnros, M. Frischholz, K. Rottner, N. Nordell, S. Karlsson, and V. Grivickas, "Investigation of Surface Recombination and Carrier Lifetime in 4H/6H-SiC," *Material Science and Engineering B61-62*, pp. 239-243, 1999.
- [4] T. Kimoto, N Miyamoto, and H. Matsunami, "Performance Limiting Surface Defects in SiC Epitaxial p-n Junction Diodes," *IEEE Trans. on Electron Devices*, vol. 46, pp. 471-477, Mar. 1999.
- [5] S. Ryu, A. K. Agarwal, R. Singh, and J. W. Palmour, "1800V NPN Bipolar Junction Transistors in 4H-SiC," *IEEE Eletron.Device Lett.*, vol. 22, pp. 124-126, Mar. 2001.
- [6] V. A. K. Temple, "Junction Termination Extension (JTE), A New Technique for Increasing Avalanche Breakdown Voltage and Controlling Surface Electric Fields in P-N Junctions," in *IEDM Technical Digest*, pp. 423-426, 1977.
- [7] C. Huang and J. A. Cooper, Jr., "4H-SiC Bipolar Junction Transistors with $BV_{CEO} > 3,200V$," *Proceedings ISPSD*, pp. 57-60, 2002.
- [8] S. M. Sze, *Physics of Semiconductor Devices*, 2nd Ed., Wiley, 1981, pp. 14

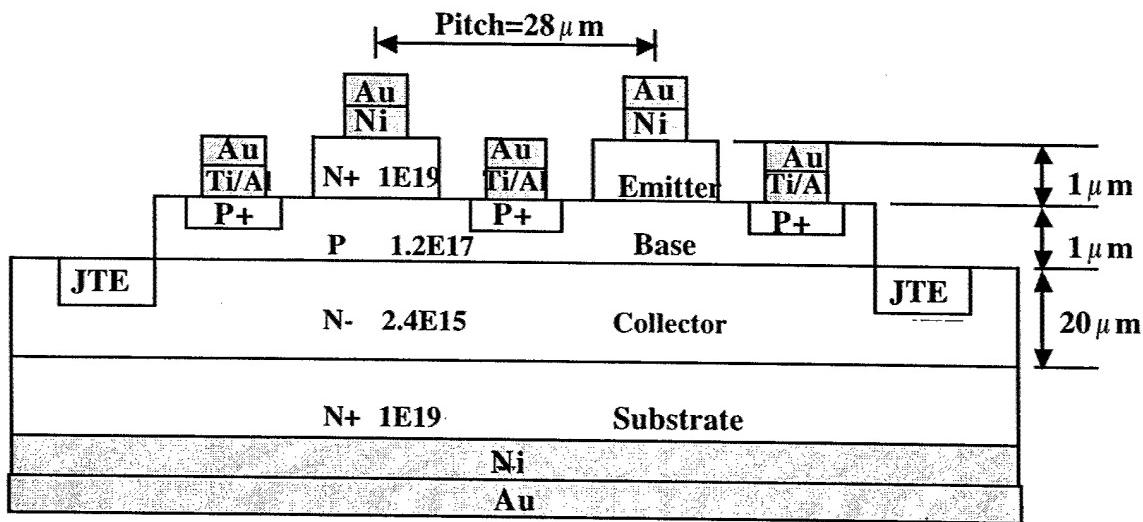


Figure 1. A schematic cross section view of the 4H-SiC BJT.

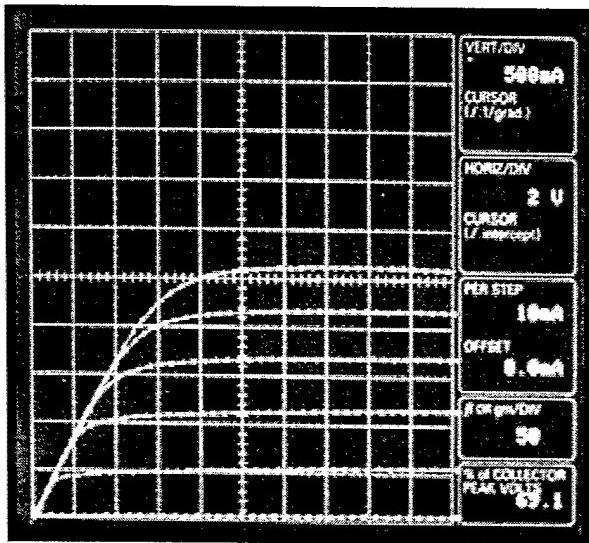


Figure 2. On-state characteristics of a 4H-SiC BJT with active area of 1.05 mm^2 and finger length of $350\mu\text{m}$. The horizontal division is 2V . The vertical division is 500mA . The base current increment is 10 mA .

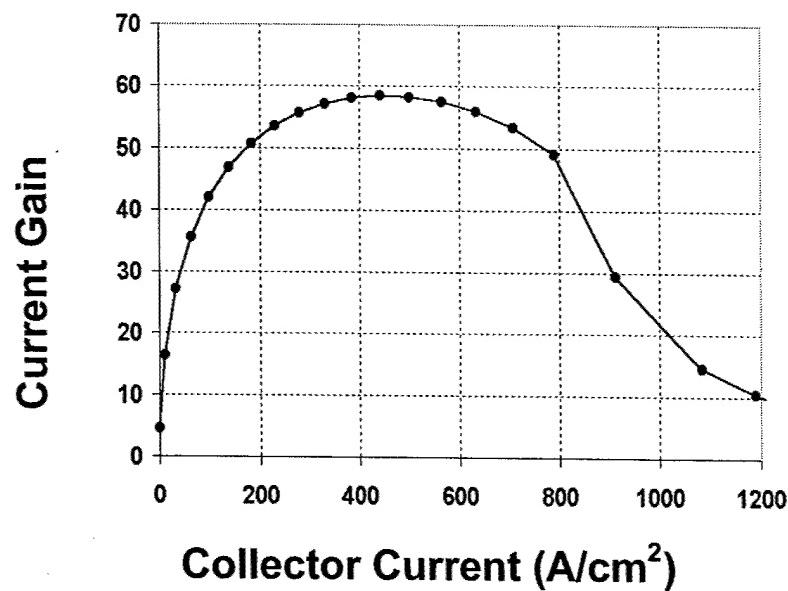


Figure 3. Current gain β versus collector current density J_C of a small BJT with active area of $55 \times 55 \mu\text{m}^2$.

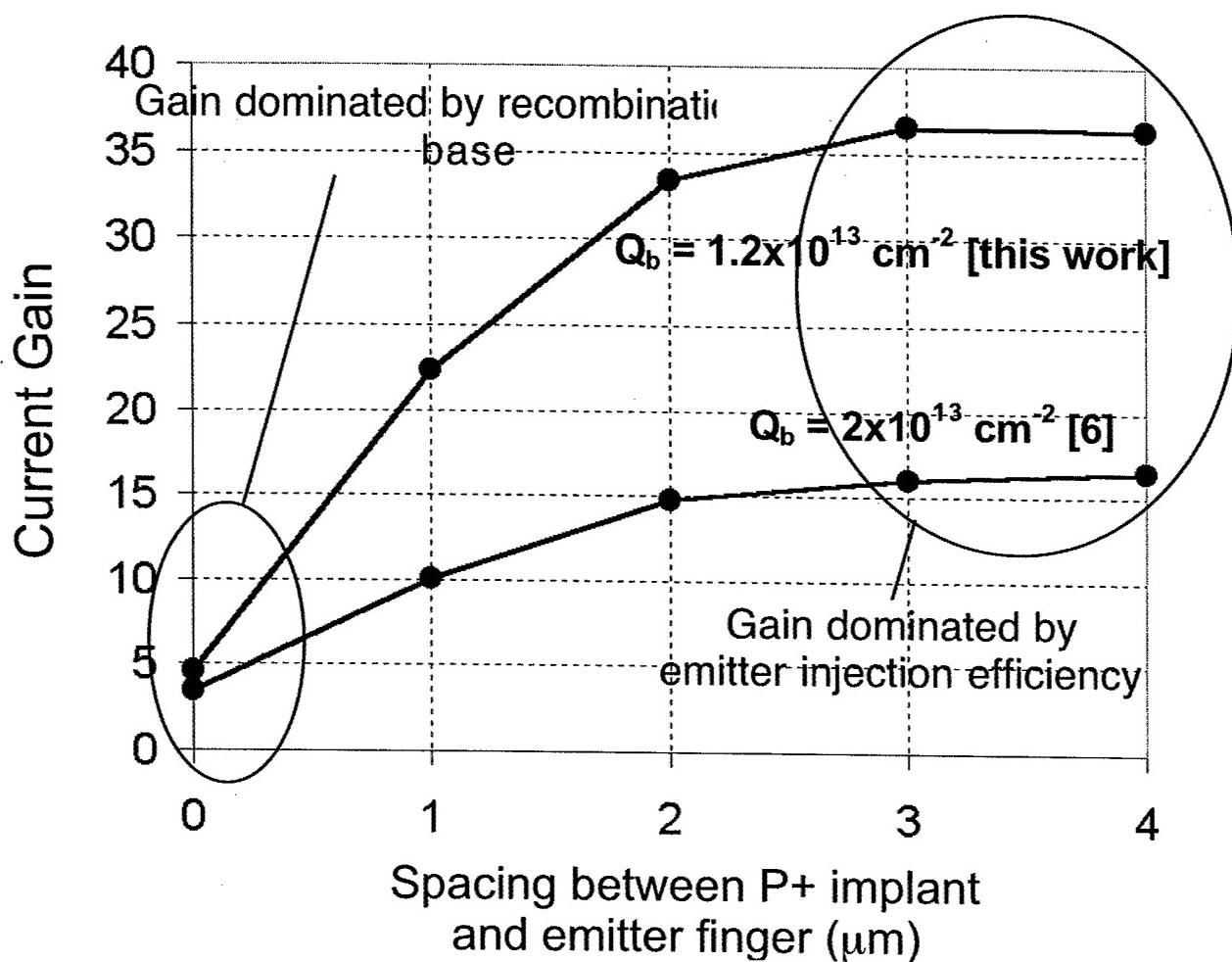


Figure 4. Dependence of current gain on (i) base dose and (ii) the spacing between the p+ base contact implant and the edge of the emitter finger. For spacings above 3 μm , the current gain is determined by emitter injection efficiency, and is inversely proportional to base dose. For spacings below 1 μm , the current gain is limited by recombination at the base contact implant.

3. Bipolar Junction Transistors in 4H-SiC with $BV_{CEO} > 3,200$ V

Device Design and Fabrication

In this work, both emitter and base layers are formed by epitaxy, so the emitter and base widths are well controlled. In addition, the carrier lifetime is expected to be longer in an epilayer than in an implanted region. These devices have an interdigitated finger structure to minimize current crowding due to the lateral resistance of the base layer. Single zone junction termination extension (JTE) is used to reduce field crowding at the device periphery in the blocking state [4].

Bipolar transistors are fabricated in n+/p/n- epilayers on the (0001) surface of a conducting n+ 4H-SiC substrate cut 8° off axis. The top n+ emitter layer is 1 μm thick, doped above 1×10^{19} cm⁻³ with nitrogen; the p-type base layer is 1 μm thick, doped 2×10^{17} cm⁻³ with aluminum; and the n- collector layer is 50 μm thick, doped 8×10^{14} cm⁻³ with nitrogen. Emitter fingers are defined by reactive ion etching in SF₆. P+ base contact regions are formed along each base finger by implantation of aluminum at 650 °C at dose/energies of $6 \times 10^{13}/40$ and $1.6 \times 10^{14}/130$ (cm⁻²/keV). The JTE ring is formed by a second aluminum implantation at 650 °C and dose/energies of $1 \times 10^{12}/40$, $2 \times 10^{12}/100$, $3 \times 10^{12}/200$, and $5 \times 10^{12}/350$ (cm⁻²/keV). Both implants are activated by annealing at 1600°C for 30 minutes in argon. The implant activation percentage is estimated to be 70%. After an RCA clean, an MOS-quality oxide is thermally grown in wet O₂ at 1150°C for 2.5 hours to passivate the surface. P-type base ohmic contacts are composed of 30 nm titanium followed by 100 nm of aluminum, and n-type emitter and back side contacts are 100 nm of nickel. All contacts are annealed at 1000°C for 2 minutes in argon. A 0.5 μm gold layer is deposited on the back, and a 0.8 μm gold layer is deposited as top interconnecting metal. A cross-sectional view of the device is shown in Fig. 1.

Results and Discussion

Current-voltage curves of the fabricated devices are extracted using an HP-4156 semiconductor parameter analyzer and a Tektronix 371A curve tracer. The high voltage performance is measured with samples immersed in Fluorinert. Elevated temperature measurements are performed on a hot chuck.

The n-type and p-type contacts are ohmic after anneal, with specific contact resistivities of 2×10^{-5} and $1 \times 10^{-3} \Omega\text{-cm}^2$ at room temperature, as determined from TLM measurements. Although the p-type contact resistance is higher than the n-type, the estimated additional voltage drop due to the contact resistance is less than 0.1 V, which is small compared with the built-in potential of the emitter-base junction. Therefore the effect of p-type contacts on device performance can be neglected.

Figure 2 shows the on-state characteristics of a large device with active area = 1.05 mm^2 (finger length = $350 \mu\text{m}$) at room temperature. The device carries 1.2A (115 A/cm^2) at a forward voltage of 11.5 V and a base current of 80 mA . DC current gain is 15. The specific on-resistance is $78 \text{ m}\Omega\text{-cm}^2$, about 1.9 times higher than the theoretical unipolar value for this epilayer. Figure 3 shows that BV_{CEO} is greater than $3,200 \text{ V}$, about 40% of the theoretical value for a one-sided step junction on this n-type epilayer. The figure of merit $V_B^2/R_{\text{ON,SP}}$ is 131 MW/cm^2 , comparable with the best SiC MOSFETs reported to date [5, 6].

Figure 4(a) shows the on-state characteristics of a small device with active area of 0.0072 mm^2 (finger length = $60 \mu\text{m}$) at room temperature. The device maintains a current gain greater than 20 up to a collector current of 300 A/cm^2 at a V_{CE} of 10 V . Above this current density, the device enters saturation, and the current gain is reduced because the base-collector junction is forward biased. $R_{\text{ON,SP}}$ is $28 \text{ m}\Omega\text{-cm}^2$, smaller than the theoretical unipolar value. This can be explained by lateral spreading of current in the thick collector in the small size devices, and conductivity modulation in the collector region. From Fig. 4(b), the ideality factor for base current η_B is close to 2, indicating the base current is dominated by recombination. The collector

current, on the other hand, is dominated by $\eta_C = 1$ diffusion current. The power dissipated in driving the base current of the small BJT is only about 2% of its total on-state power loss.

The dependence of current gain on the gap “d” between the p+ base contact implant and the emitter edge (see Fig. 1) is shown in Fig. 5. As the base contact implant is brought closer to the emitter edge, the current gain decreases monotonically. It is likely that the p+ implant introduces defects that are not completely removed during the activation anneal. As the implanted region is brought within an electron diffusion length of the emitter edge, recombination at these defect sites reduces the current gain. $R_{ON,SP}$ increases and β decreases with operating temperature, consistent with observations of other groups [2, 3].

Conclusions

4H-SiC npn BJTs are fabricated on 50 μm n-type epilayers. An open-base blocking voltage BV_{CEO} of 3,200V is achieved, the highest value reported to date for SiC BJTs. Large devices exhibit a common emitter current gain of 15 and a specific on-state resistance of 78 $\text{m}\Omega\cdot\text{cm}^2$. Small devices exhibit a current gain around 20. The figure of merit $V_B^2/R_{ON,SP}$ is 131 MW/cm², comparable with the best reported SiC MOSFETs. A parallel study indicates that the spacing between p+ base contact implant and the edge of the emitter has a strong effect on current gain. This is attributed to recombination at defect sites within the implanted p+ region.

References

- [1] A. Huang, and B. Zhang, “The Future of Bipolar Power Transistors,” *IEEE Trans. on Electron Devices*, vol. 48, pp. 2535-2543, Nov. 2001.
- [2] S. H. Ryu, A. K. Agarwal, R. Singh, and J. W. Palmour, “1800V NPN Bipolar Junction Transistors in 4H-SiC,” *IEEE Electron Device Lett.*, vol. 22, pp. 124-126, Mar. 2001.
- [3] Y. Tang, J. B. Fedison, T. P. Chow, “An implanted-Emitter 4H-SiC Bipolar Transistors with High Current Gain,” *IEEE Electron Device Lett.*, vol. 22, pp. 119-120, Mar. 2001.

- [4] D. Sheridan, G. Niu, J. N. Merrett, J. D. Cressler, J. B. Dufrene, J. B. Casady, and I. Sankin, "Comparison and Optimization of Edge Termination Techniques for SiC Power Devices," *Proc. 13th Int. Symp. On Power Semiconductor Devices and ICs*, pp. 191-194, 2001.
- [5] I. A. Khan, J. A. Cooper, Jr., M. A. Capano, T. Isaacs-Smith, and J. R. Williams, "High-Voltage UMOSFETs in 4H-SiC," *International Symposium on Power Semiconductor Devices*, Santa Fe, NM, June 3 -7, 2002.
- [6] Y. Sugawara, K. Asano, D. Takayama, S. Ryu, R. Singh, J. Palmour, and T. Hayashi, "5.0 kV 4H-SiC SEMOSFET with Low RonS of 88 mΩ cm²," *Mat'l Sci. Forum*, Vols. 389-393, pp. 1199-1202, Trans. Tech. Publications, Sweden, 2002.

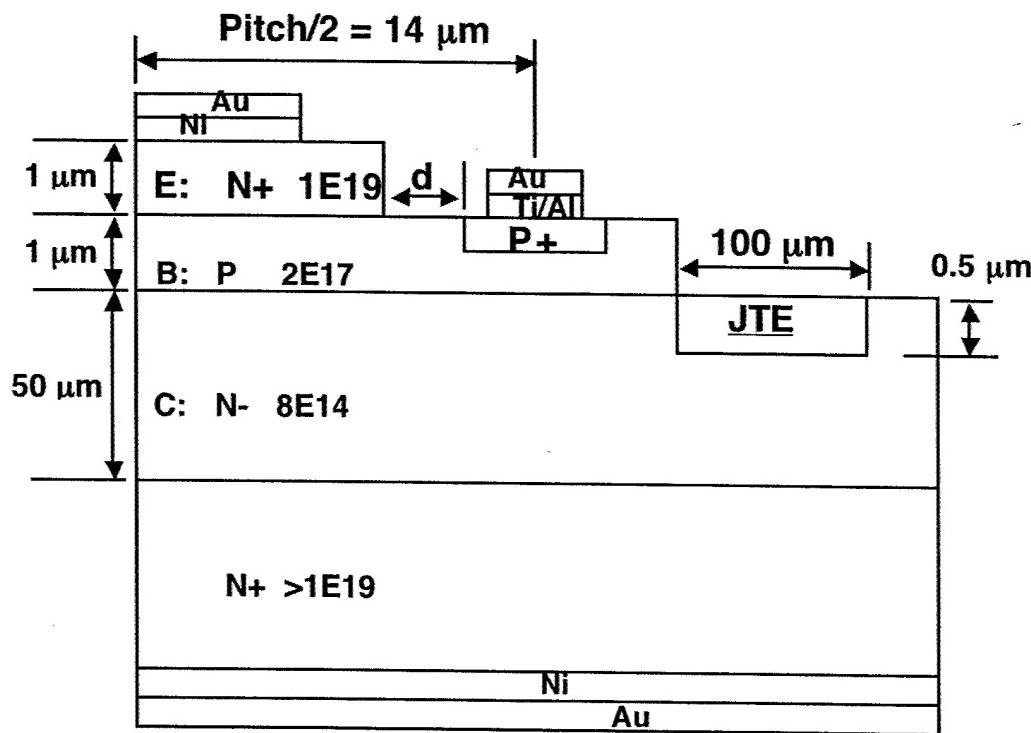


Figure 1. Schematic cross section of the 4H-SiC BJTs. Note the critical dimension "d" between the edge of the emitter and the edge of the P+ base contact implant. This dimension is critical to achieving high current gain, as discussed in Section 2.

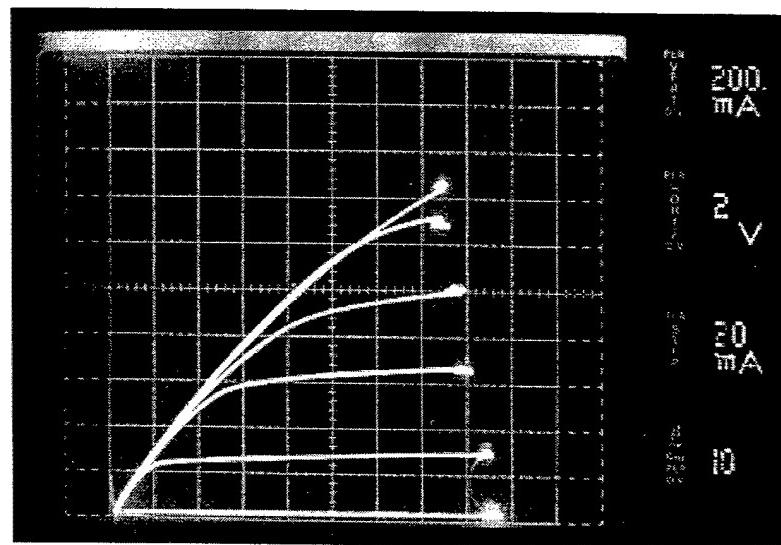


Figure 2. On-state characteristic of the large BJT (active area = 1.05 mm²) at room temperature.

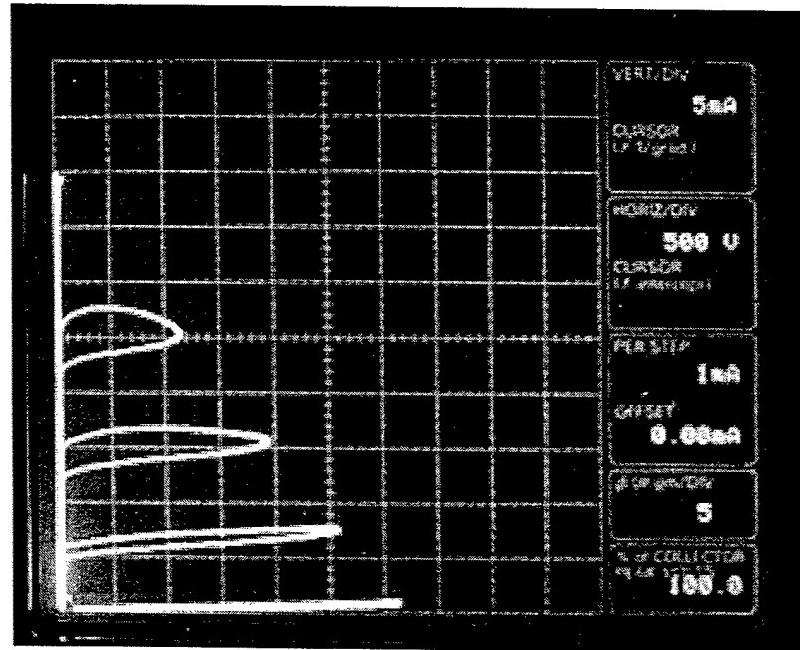
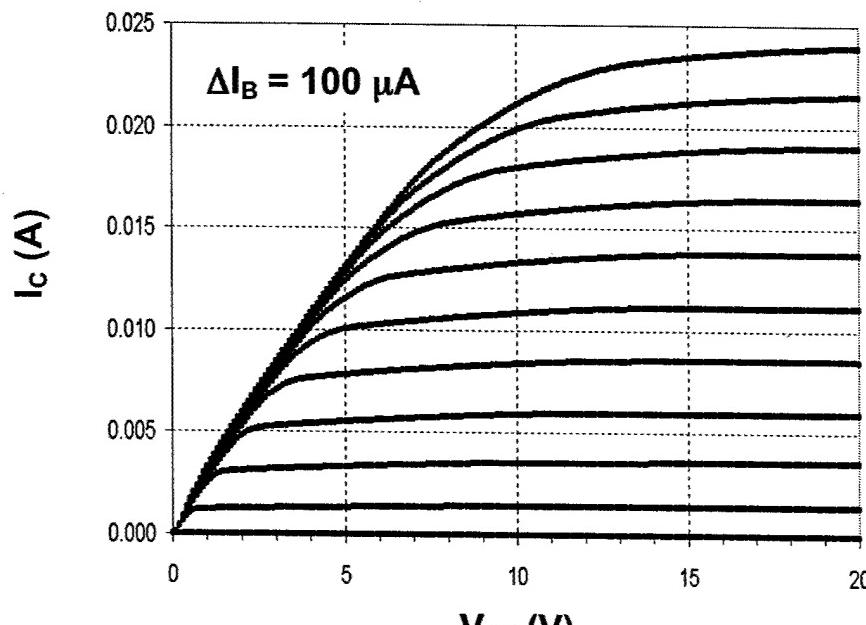
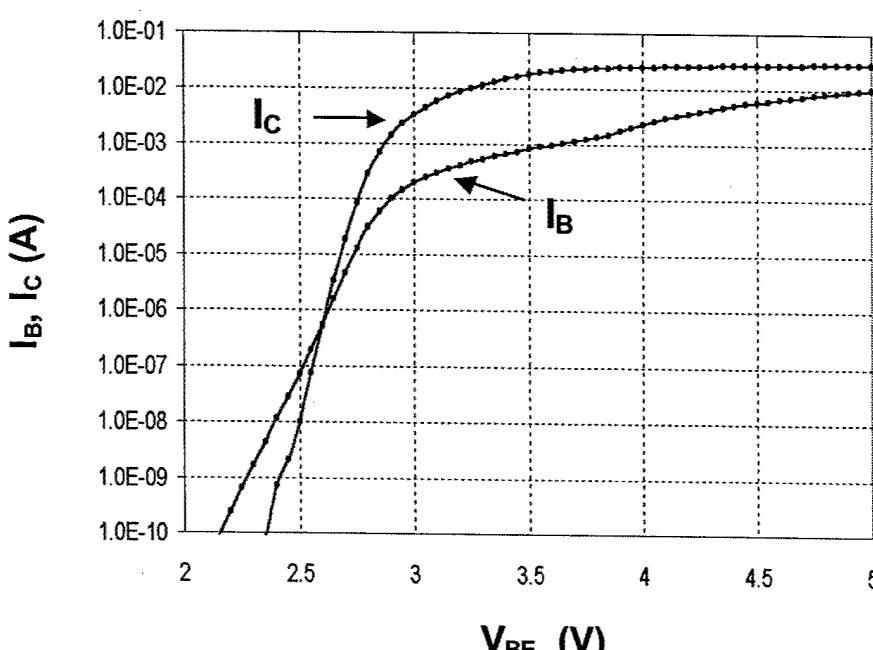


Figure 3. Blocking characteristic of the large BJT ($V_{CEO} > 3,200V$).



(a)



(b)

Figure 4. On-state characteristics of the small BJT (active area = 0.0072 mm^2) at room temperature. (a) I-V curves, (b) Gummel plot at $V_{CE} = 10 \text{ V}$.

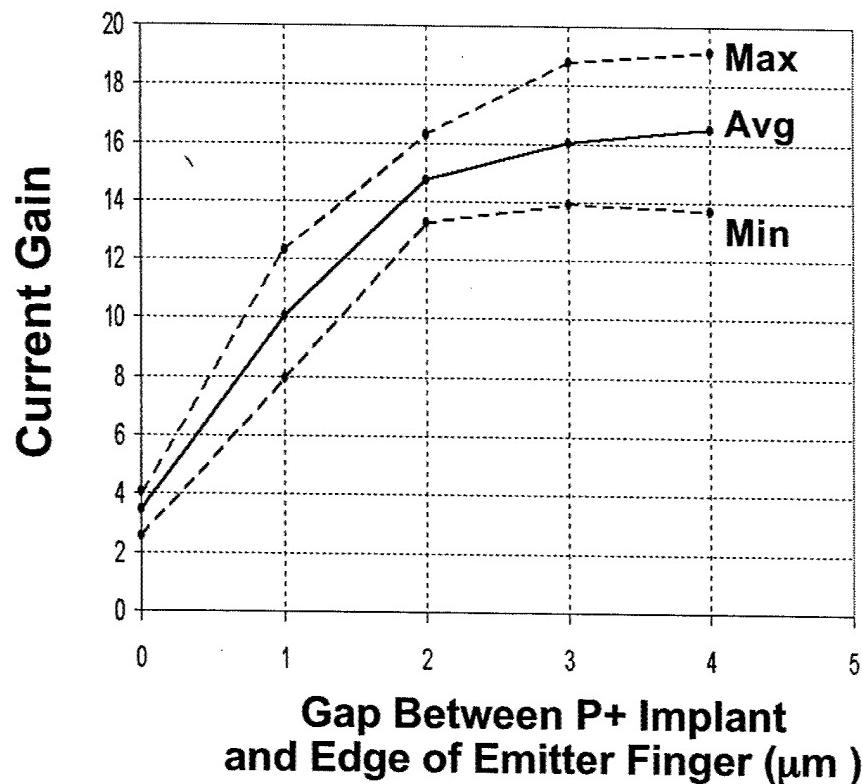


Figure 5. Current gain of the small BJT as a function of spacing "d" between the p-type base contact implant and the edge of the emitter.